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A bus on a diet-the serial bus alternative-an introduction to the P1394 High Performance Serial Bus

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Abstract

The author discusses the justifications for the use of a serial bus in computer systems. He then describes a leading proposal for such an interconnect: the IEEE P1394 High Performance Serial Bus. The highlights of the Serial Bus include: (1) a physical layer supporting both cable media and many ANSI/IEEE standard 32-bit buses; (2) variable speed data transmission with a base speed of almost 100 Mbit/sec between nodes separated by distances up to 10 meters; (3) both fair and priority arbitration mechanisms with all nodes guaranteed at least partial access to the bus regardless of priority; (4) bus transactions that include block and single quadlet reads and writes, as well as an isochronous mode which provides a low-overhead guaranteed bandwidth service; and (5) dynamic address assignment that does not require switches or a physical 'slot number'

Index Terms

Controlled Indexing
standards system buses

Non-controlled Indexing

100 Mbit/s ANSI/IEEE standard 32-bit buses IEEE P1394 High Performance Serial Bus bandwidth service base
single block quadlet reads block quadlet writes cable media dynamic address assignment fair arbitration
isochronous mode partial access physical layer priority arbitration serial bus single quadlet reads single quadlet
writes variable speed data transmission

Author Keywords

No Available

References

No references available on IEEE Xplore.

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2	<input type="checkbox"/>	<input type="checkbox"/>	US 6900812	20050531	20	Logic enhanced memory and method therefore	345/540	345/531;
			B1			and method therefore		345/537;
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6636223	20031021	20	Graphics processing system with logic enhan	345/581	345/522;
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			A			processor for controlli		711/143;
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